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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,067	07/09/2003	Toshifumi Kojima	040894-5940	7994

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EXAMINER
LAM, CATHY FONG FONG

ART UNIT	PAPER NUMBER
1775	

DATE MAILED: 11/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,067	KOJIMA ET AL.	
	Examiner	Art Unit	
	Cathy Lam	1775	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *August 10, 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-7 and 10-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-7 and 10-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

In view of the amendment and remarks filed on August 10, 2006, the pending claims continue to be unpatentable as following:

Claim Rejections - 35 USC § 103

1. Claims 5-7 and 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa et al (US 5243142) in view of Nakatani et al (US 6108903) further in view of Kambe et al (US 6323439).

Ishikawa discloses a printed wiring board comprised of an insulating substrate (1), via hole (3), electroconductive plating (4), a filing material and a second plating layer (6) (Figs. 2 & 3).

Via hole (3) is formed through the thickness of the insulating substrate and an electroconductive plating layer (4) is plated on the wall of the via hole (3) (col 1 L 66-68). The via hole is then filled with a non-electroconductive resin paste which is comprised of metal powder having diameter of 0.3 to 10 μm and a thermosetting resin (col 3 L 14-17). A second plating layer is plated over both surfaces of the cured resin paste (col 2 L 1-6). The second plating layer (6) is a conductive layer (col 3 L 52-55).

The examiner is taking the position that the metal powder is the filler of the non-conductive resin paste.

Ishikawa further teaches that the invention can be applied to a multilayer printed circuit board (col 4 L 35-37).

Ishikawa does not go into details about the ingredients of the non-conductive paste layer nor does it teach the diameter of via hole.

Nakatani teaches a conductive paste which is used in a connecting member that couples with circuit substrates. The conductive paste is comprised of conductive fillers, a thermosetting resin, a curing agent (or hardener) and a curing catalyst.

The conductive paste is used to fill the through holes of the connector member; the through holes have a diameter from 50 μm to 1 mm, more preferably from 100 μm to 300 μm (col 7 L 38-41). The conductive fillers have an average particles size range from 0.2 to 20 μm (col 9 L 34-35). The fillers are dispersed in the thermosetting resin which is a solvent free epoxy resin liquid (col 9 L 59-63).

The hardener used in the conductive paste can be dicyandiamide and an urea hardener such as 3-(3,4-dichlorophenyl)-1,1-dimethyl urea (col 10 L 19-22). Nakatani further teaches that the hardener is in the form of powder (col 10 L 27-28).

Nakatani teaches all the ingredients for the conductive paste, but is silent about the hardener's (or curing agent) particle size.

In view of Nakatani's teaching, the examiner is taking the position that one of ordinary skill in the art would choose a size range that is most optimum to his invention because such discovery involves only routine experimentations.

Regarding to the structure of the present invention, Kambe teaches a multilayer printed wiring board comprised of a surface wiring board and a core wiring board (Fig. 3F).

The surface wiring board is comprised of an insulating layer with through holes and conductive pattern layer (71). The conductive pattern layer is formed onto the surface of the insulating layer and on the wall of the through holes (63).

The surface wiring board is placed over the core wiring board that has plated via holes connect to the conductive pattern layer (71) in the surface wiring board (Fig. 1). The via holes (H4) in the core wiring board has a diameter of 50 μm (col 7 L 60-61).

In view of the prior art teachings, one skill in the art would fabricate a multilayer printed circuit board that has a plated through holes filled with a conductive paste or a non-conductive paste, and having a second conductive layer over the filled via hole for connecting to another wiring board because such structure is well known in the circuit board field. Furthermore, the conductive paste having the claimed ingredients are well known in the conductive composition art.

Response to Arguments

2. Applicant's arguments filed on August 10, 2006 have been fully considered but they are not persuasive. Applicant in the remarks argues what *each* of the three prior art lacks, the examiner is taking the position that the rejection is based on a combination of all three prior art together which is obvious over the present invention.

3. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cathy Lam whose telephone number is (571) 272-1538. The examiner can normally be reached on 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jennifer McNeil can be reached on (571) 272-1540. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cathy Lam
Primary Examiner
Art Unit 1775

cfl
November 07, 2006